Comparison of Decimation Filter Architectures for a Sigma-Delta Analog to Digital Converter

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***Abstract*— Different decimation filter architectures are compared for integration with an existing second order sigma-delta modulator to form a sigma-delta ADC. The decimation filters are implemented using a third order cascaded integrator comb filter programmed to work for oversampling ratios of 64, 128 and 256. IIR-FIR, non-recursive and polyphase architectures of decimation filters are simulated and implemented using 130nm CMOS technology. Pros and cons of different architectures are compared using parameters like area, power consumption and potential for future technologies.**

***Index Terms*— ADC, sigma-delta, decimation filter, Cascaded Integrator Comb.**

I. Introduction

Over the last three decades there were tremendous developments going in the area of digital signal processing supported by the development of integrated circuits. Since most of the signals in this world are analog, they need to be converted to digital form for processing. This is done with the help of Analog to Digital converters. Different types of analog to digital conversion techniques are available today, each having its own advantages and disadvantages. Comparing with different ADC architectures, sigma-delta ADC provides high resolution in low and medium frequencies which makes them suitable for medical application and audio application.

A sigma-delta A/D converter consists of two parts: an analog oversampled modulator and a digitally implemented decimation filter [1]. The decimation filter relaxes the requirement of high precision analog circuits in the modulator stage and increases the output resolution of ADC. A second order sigma-delta modulator integrated with a third order decimation filter to form a sigma-delta ADC is simulated in SIMULINK® with MATLAB® as the computing software package. The 1-bit output of the modulator is used as the input to different decimation filter architectures implemented in 130nm CMOS technology. Each decimation filter architecture implementation include RTL-description, synthesis and post-synthesis result comparion with the simulated Matlab results. Post-synthesis power dissipation is computed with Synopsys® Power Compiler.

II. Decimation filter architectures

An economical hardware implementation of a multistage decimation filter can be done using Cascaded Integrator Comb filter (CIC) with the transfer function [2]

$$H(z) = \left(\frac{1 - z^{-N}}{1 - z^{-1}}\right)^k \tag{1}$$

where N is the oversampling ratio and k is the order of the filter (k=3). Figure 1 shows the direct

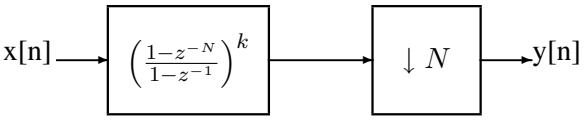

Fig. 1. Direct implementation of CIC filter

implementation of decimation filter. Since the whole circuit is working at sampling frequency, f_s ($f_s = N \cdot Nyquistrate$) the power consumption of the circuit is high [3]. So different decimation filter architectures are required.

A. IIR-FIR structure

A simplified implementation of CIC filter is shown in Fig. 2. In this circuit, the IIR filters work at f_s and the FIR filter works at Nquist rate (f_N). So the power consumption of this architecure is reduced significantly. Moreover the area is reduced due to the

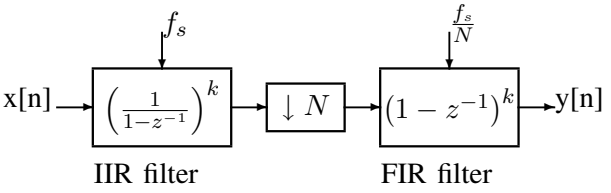

Fig. 2. Block diagram of IIR-FIR decimation filter structure

reduction of registers and adders. To avoid register overflow the word length of the IIR filter should be $b + k \cdot log_2 N$, where b is the length of the output of modulator (here $b = 1$) [3].

B. Non-recursive structure

The transfer function of the comb decimation filter given by eq. (1) can be simplified as eq. (2)

$$H(z) = \prod_{i=0}^{(\log_2 N)-1} (1 + z^{-2^i})^k \tag{2}$$

This decimation filter can be realized using a cascade of $\log_2 N$ FIR filters of order $k \cdot 2^i$ where i=0 to i=[$(\log_2 M)$ - 1], succeeded by the down-sampler [3]. This structure is called 'non-recursive structure' because there are only FIR filters needed for implementation while in IIR-FIR structure is a recursive one due to IIR filters. So there are no stability related issues in non-recursive structure.

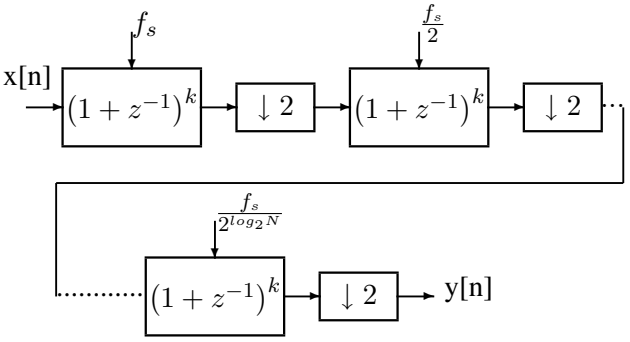

Fig. 3. Block diagram of non-recursive decimation filter structure

TABLE I
PARAMETERS OF STAGE i IN NON RECURSIVE STRUCTURE[$i = 1, 2..(\log_2 M)$]

	Input	Output
Sampling rate	$\frac{f_s}{2^{i-1}}$	$\frac{f_s}{2^i}$
Wordlength	$b + k \cdot (i-1)$	$b + k \cdot i$

The input x[n] is the output of sigma-delta modulator whose wordlength is b bits (b =1). The wordlength increases by k bit through every stage while the sampling rate decreases by a factor of 2 starting from f_s. Reducing sampling rate in the earlier stages helps to reduce the power consumption.

C. Polyphase structure

In the non-recursive structure the output is decimated by factor 2, implies that half of the output is not used. This leads to waste of computational resources and increased power consumption. By applying polyphase decomposition we can get a more efficient implementation. Each FIR filter in non-recursive structure can be implemented by 2-component polyphase decomposition of its transfer function [3].

$$H(z) = (1 + z^{-1})^k = H_0(z^2) + z^{-1} \cdot H_1(z^2) \tag{3}$$

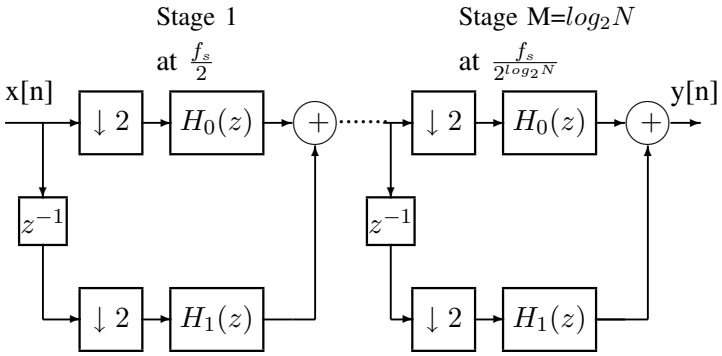

Fig. 4. Block diagram of polyphase decimation filter structure.

In this work we are using filter of order k=3. So the eq. (3) become
$H(z) = (1 + z^{-1})^3 = 1 + 3z^{-1} + 3z^{-2} + z^{-3}$
$= 1 + 3z^{-2} + z^{-1}(3 + z^{-2})$
where $H_0(z)$,$H_1(z)$ are given as

$$H_0(z) = (1 + 3z^{-1}) \tag{4}$$

$$H_1(z) = (3 + z^{-1}) \tag{5}$$

This is implemented in Fig. 4. This structure allows the placement of the downsamplers at the input of the filter, making the whole structure work at half the frequency it used to work in non-recursive structure at the cost of increased circuitary.

III. Results and Comparison

These structures are implemented in Verilog and synthesized using 130nm CMOS technology. Synopsys® Design Compiler is used for synthesis. All the decimation filter architectures are implemented for oversampling ratio's of N=64,128,256. Post synthesis results are compared with the sigma-delta ADC design in Matlab®.

A. Area

From Fig. 5 we can see that the area is least in case of IIR-FIR structure, increases with non-recursive structure and the highest in polyphase structure for the same oversampling ratio.

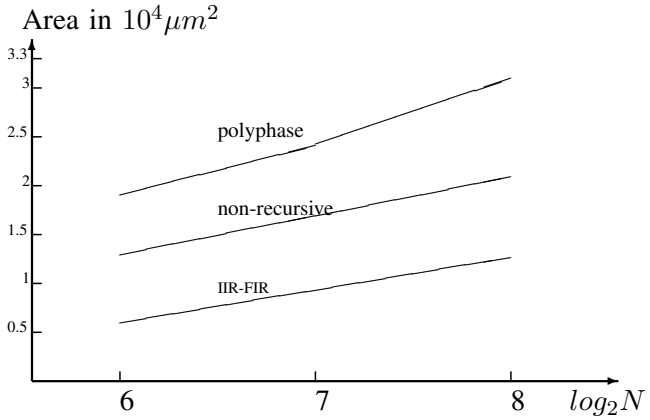

Fig. 5. Comparison of area for different decimation architectures.

TABLE II
AREA (μm^2) FOR DIFFERENT DECIMATION FILTER STRUCTURES

Oversampling ratio	IIR-FIR	Non-recursive	Polyphase
64	6648	12951	19080
128	7635	16555	24807
256	8591	20638	31077

IIR-FIR structure has minimum area for a given oversampling ratio and the increase in the area with oversampling ratio is minimum compared to other structures. Moreover the increase in area with oversampling ratio remains the same. For an increase of oversampling by 2 the IIR and FIR register wordlength should be increased by 'k' (order of filter, k=3). Increase in area with doubling of oversampling ratio is the addition of $(2k^2+1)$-bit adder and $(2k^2+1)$-bit register.

For non-recursive structure, an additional filter block $(1+z^{-1})^k$ is added for doubling the oversampling ratio. The wordlength of this block is increased by 'k' compared to previous block. This means an increase of k-registers and k-adders of wordlength $b+k \cdot log_2 N$. So there is an increase in area between two adjacent oversampling ratio's with increasing in oversampling ratio.

Polyphase structure requires highest area compared to the other two structures. Compared to the non-recursive structure this circuitry has an extra multiplier circuit whose size increases by 'k' for the addition of the new block. So the area depends on how the multiplier is implemented. Added new block has 5 new registers and a multiplier of wordlength $b + k \cdot log_2 N$. So this structure has a non-linear increase in area with increase in oversampling ratio.

B. Power consumption

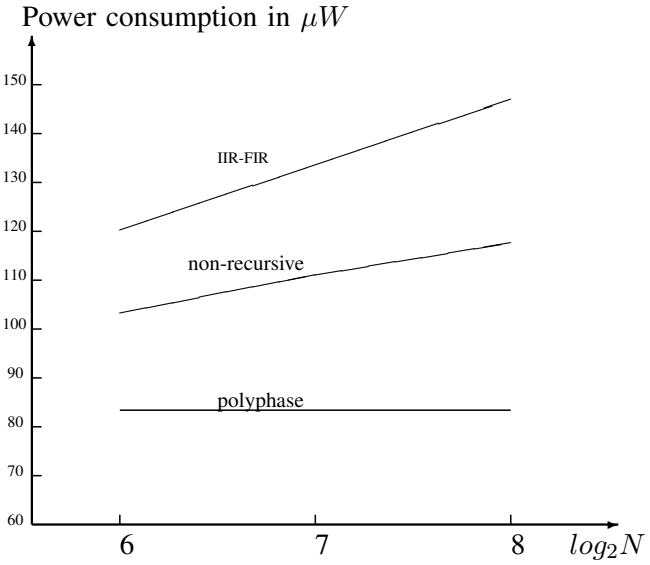

Fig. 6. Comparison of power consumption for different decimation architectures.

TABLE III
POWER (μW) FOR DIFFERENT DECIMATION FILTER STRUCTURES

Oversampling ratio	IIR-FIR	Non-recursive	Polyphase
64	120.3	103.2	83.4
128	136.7	110.4	84.6
256	152.51	113.7	85.6

From the comparison shown in Fig. 6, Polyphase structure has the minimum power consumption followed by non-recursive structure and worst in case of IIR-FIR structure. The increase in power consumption between two consecutive oversampling ratios for IIR-FIR structure is linear. The newly added bits of FIR block work with Nyquist frequency while that of IIR stage works at double the frequency compared to the previous oversampling ratio. There is no dependence of increase of wordlength on oversampling ratio, so the power consumption increase remains the same between two consecutive oversampling ratios.

For a non-recursive structure, the newly added blocks for higher oversampling rate works at half frequency and increased wordlength. The increase in power is non-linear because there is a dependence of increased wordlength on oversampling ratio. Power

consumption is directly proportional to frequency. So with higher oversampling ratio's the increase in power consumption between two adjacent oversampling ratios will decrease.

Polyphase structure has the least power consumption of all other structures. The advantage of this structure increase in power consumption between two adjacent oversampling ratios is less than that of non-recursive structure for the same oversampling ratios. This is due to downsampling occurs first followed by filtering. So the downsampling registers work with frequency of the block while the filter registers work with half the frequency. Remember that with every block the frequency decreases in the same way it decreases in non-recursive structure.

C. Potential for future technologies

An oversampled ADC is mainly used at low and medium frequency domain. In sensor application, ADC should be integrated with the sensor and low power consumption is required for battery lifetime. Although IIR-FIR structure has the least area, the linear characteristic of power make them unsuitable for future applications. Future applications require high resolution achieved by increase in oversampling ratio, increases the power consumption of IIR-FIR structure to a high level making them incompatible for future chips.

Polyphase decomposed structures are more probable in future application, but it has a disadvantage of increased area with higher filter order and resolution. With the development of new technoloy the dimensions of a transistor is reduced, so area won't be a constraint. Power will be compromised for area in future application since developing chips are aimed to work at low power. But for an efficient implemenation of a polyphase structure, multiplier should be implemented using Wallace Tree [4]. But when size for integration in a chip become a constraint mostly people will prefer non-recursive structure because of its ease of implementation and good power to area optimization for higher filter orders and oversampling ratios.

IV. Conclusions

This paper described about different decimation filter architectures (IIR-FIR, non-recursive and polyphase structures). Comparison of these architectures with parameters like area, power consumption and future use is done by implementing them in 130nm CMOS technology. It can be concluded that polyphase decimation filters have more future use because of its low power consumption with increasing oversampling ratios, although its performance in area and ease of implementation is not good compared to other two decimation filter structures.

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