An opamp array test structure for stress test measurements

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Abstract

This paper is about setting up of an opamp array test structure for investigating the degradation of differential amplifier circuit performance and variation of its individual transistor parameters in a stress test. In an analog circuit implemented using transistors with ultra-thin gate dielectric oxide, the increased gate leakage current results in the increased chances of transistor dielectric breakdown and effects significantly the circuit performance. Differential amplifiers with transistors having t_{ox}=2.2 nm are designed for applying voltage and temperature stresses. Transmission gates and other logic circuitry transistors with oxide thickness 6.5 nm are used to stress the differential amplifier circuit and to address individual transistors in the differential amplifier circuit. An array of 16 differential amplifiers with transmission gates are implemented for stress test measurements.

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1. Introduction

The increase in gate leakage current and oxide dielectric breakdown are the challenges accompanied with the aggressive scaling of gate oxide thickness. Time Dependent Dielectric Breakdown (TDDB) testing is the standard methodology for developing transistor operating lifetime reliability projections. It is performed under constant voltage stress, constant current stress, temperature stress or a combination of these stresses on transistors until failure is observed [1]. Two breakdown regions namely soft breakdown (SBD) and hard breakdown (HBD) are categorized according to magnitude of post breakdown gate current.

In ultra-thin gate oxides (t_{ox}<5 nm), soft breakdown is the major area of focus in research. This is due to the variations in transistor parameters such as threshold voltage (V_{th}), gate current (I_g) and transconductance (g_m) in a circuit are shifted more than the tolerances set by the corner simulation (process window). From the paper by Ogas et al. [2], it can be seen that the variation of the parameters in an inverter circuit is more than the corner window provided by a circuit simulation in soft breakdown region. Traditional approach [3] is to wire a stressed transistor into an ideal circuit and to measure the performance of the circuit. But we cannot assure that mismatch in identical transistors parameters due to stress are same. So it became important to stress a differential amplifier as a whole in order to see the variation of parameters of the differential amplifier circuit in different breakdown regions and see how the variations of individual transistors affect the differential amplifier performance.

In this work, an array of 16 differential amplifiers is implemented so that it can be stressed individually and each transistor in the differential amplifier circuit can be addressed outside for stressing and measurement. Differential amplifiers to be stressed are implemented using transistors having t_{ox}=2.2 nm and the rest circuitry for stressing and addressing with transistors of t_{ox}=6.5 nm so that the stress voltage wont degrade the addressing transistors.

2. Opamp test structure

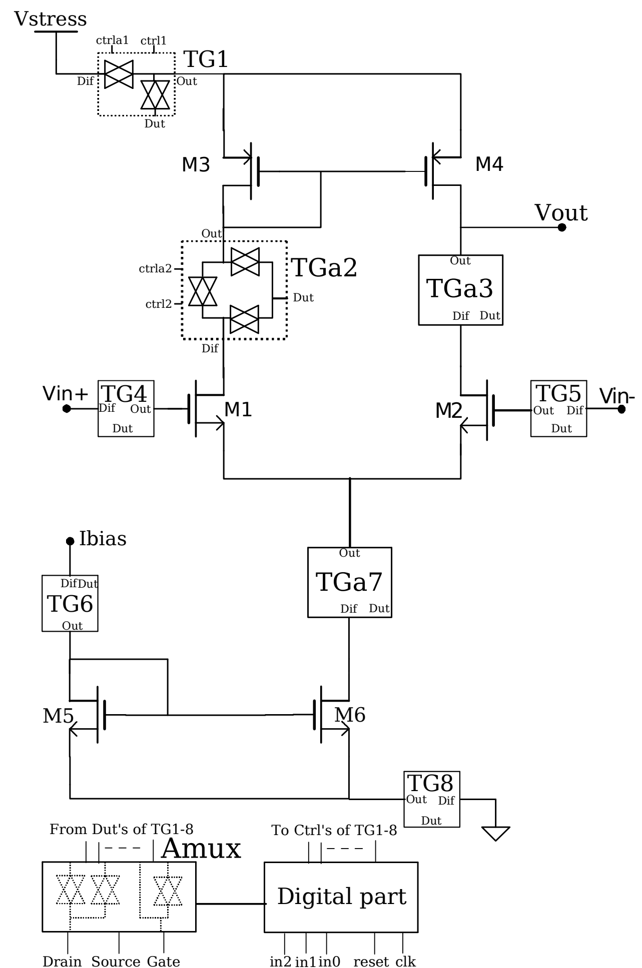

Fig. 1 Opamp test structure.

The differential amplifier is the input stage of a widely used Miller Opamp [4] having a differential input and a current mirror load. This differential amplifier is implemented using 1.2 V 130 nm CMOS technology having gate oxide thickness, t_{ox}=2.2 nm. Differential amplifier is designed to give a gain of 40 dB, common mode voltage of 0.8 V and bandwidth of 60.68 kHz for a capacitive load of 10 pF.

Two blocks namely TG and TGa consisting of CMOS transmission gates are used for addressing and stressing individual transistors of the differential amplifier circuit are implemented using transistors having t_{ox}=6.5 nm for a supply voltage of 3.3 V. An optimum value of W/L-ratio of transistors is decided so that the variation between the differential amplifier with and without transmission gates is minimum. Here we are using W=33 µm, L=500 nm for transmission gates and W=1 µm, L=500 nm for the logic gates (CMOS inverter). The variation circuit parameters such as gain and bandwidth for the differential amplifier with and without transmission gates are less than 1.5%.

The Amux-block consists of 6 CMOS transmission gates to address only the terminals of the selected transistor according to the given digital input from the 'Digital part' of the circuit. The layout of the opamp test structure shown in Fig. 2 is done using Cadence® Virtuoso and verified using Cadence Assura™. The dimension of the layout is 171×99 µm².

Table. 1. Truth table of opamp test structure.

in2	in1	in0	Operation
0	0	0	Stress amplifier
0	0	1	Address/Stress M3
0	1	0	Address/Stress M4
0	1	1	Address/Stress M1
1	0	0	Address/Stress M2
1	0	1	Address/Stress M5
1	1	0	Address/Stress M6
1	1	1	Circuit disconnected

An array of 16 opamp test structures and a 4×16 decoder are setup for the array test structure. When the reset of the opamp test structure is logic-0 then the differential amplifier is disconnected from stress voltage. The individual differential amplifiers can be stressed by using setting logic-1 to the reset pin and only one differential amplifier can only be stressed at a time.

3. Conclusion

An opamp array test structure is implemented for stress tests in mixed mode 130 nm CMOS technology with transistors having gate oxide thickness of 2.2 nm and 6.5 nm. The option for stressing single transistor is used to identify the critical transistors in the differential amplifier circuit. The stress test results will give an insight into the degradation of the identical transistors and the effect of their mismatch on the circuit performance. A model can be derived so that appropriate countermeasures can be taken in the future to enhance the differential amplifier circuit operating lifetime.

4. References

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[4] R. Jacob Baker, "CMOS circuit design, layout and simulation"

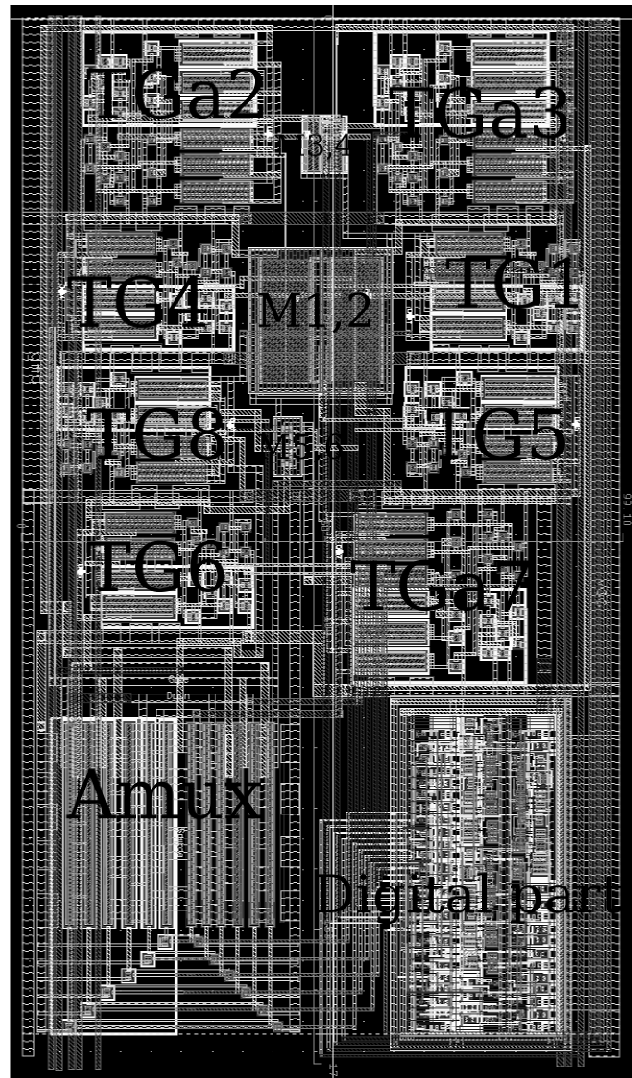

Fig. 2 Layout of opamp test structure